REMARKS

Claims 1 - 20 remain active in this application. Claims 13 - 20 have been withdrawn from consideration as being non-elected, without traverse, in response to a requirement for restriction. Claim 1 has been amended to improve antecedent language correspondence. No new matter has been introduced into the application. The indication of allowability of the subject matter of claims 8 - 12 is noted with appreciation.

While the previous election in response to a requirement for restriction was made without traverse, it was nevertheless requested in the response filed August 30, 2004, that the requirement for restriction be clarified in order to avoid possible prejudice to Applicant. No clarification has been made in the present official action and clarification in the next official action is again respectfully requested. It is respectfully submitted that an election without traverse does not relieve the Examiner of the burden of making a clear and logical statement of the necessity for such a requirement that will support avoidance of double-patenting issues in a divisional application.

The Examiner has objected to claims 8 - 12 as depending from a rejected claim but indicated that these claims would be allowable if rewritten in independent form. This objection is respectfully traversed in accordance with the traverse of the underlying rejection of claims 1 - 7 as will be set out below.

Claims 1 - 7 have been rejected under 35 U.S.C. §102 as being anticipated by Kumagai et al. This sole ground of rejection is respectfully traversed.

The invention, as recited in independent claim 1, is a method of adjusting carrier mobility in a semiconductor device by 1.) depositing a metal or combination of metals in contact with the gate of a

transistor and 2.) alloying the metal or combination of metals with the transistor gate to create a tress in the channel of the transistor. Kumagai et al. is directed to alteration of carrier mobility and provides twelve embodiments in which adjustment of carrier mobility is achieved to some degree by different structures formed by different methods. However, none of these twelve embodiments answers the method claimed.

Specifically, all embodiments include silicide films 17, 37 on the transistor gates as is common for reducing connection resistance. However, no channel stress is attributed to them. These silicide films are thin and located remote from the transistor channel where little, if any, stress developed in the silicide would or could be transferred to the transistor channel. *It is believed to be highly significant in this regard that Kumagai et al. teaches, at paragraph 0209) titanium, cobalt and nickel (among other metals) as suitable for forming such a silicide film but does not explicitly mention any development of stress in silicides by use of these metals while the present specification indicates at page 14, lines 20 - 22, that these metals are preferred for the practice of the invention due to the high or moderate stresses developed thereby. In other words, Kumagai et al. does not even recognize that stress (much less differential stresses) can be developed in gate structures by the use of these metals to form silicide, much less that it is possible to transfer such stress from the transistor gate to the transistor channel in accordance with a basic principle of the present invention.*

Rather, in most embodiments, Kumagai relies on the use of a stressed film 19 of nitride or other materials 191, 193, 391, 393 covering the gate electrode (paragraphs 0156 - 0157) to adjust transistor channel stress and carrier mobility. The only embodiments in which such a film can be omitted in accordance with

Kumagai et al. are the third, fourth, fifth, sixth and seventh embodiments. The third embodiment (in regard to which titanium cobalt and nickel are mentioned, as discussed above) provides control of stress in the transistor channel by control of thickness of silicide in the source and drain regions but not from the gate (paragraph 0214). (Again, stresses are assumed but not explicitly attributed to the silicide or silicide formation). The fourth embodiment transfers stresses from the transistor gate to the transistor channel but obtains those stresses in the gate by ion implantation of phosphorus, boron or arsenic therein rather than from silicide formation (paragraph 0219). The fifth embodiment also generates stresses in the gate but does so by the selective formation of layered and non-layered deposits of material which control grain size (paragraphs 0240 - 0242). The sixth embodiment provides control of stress in the transistor channel by developing stress in a shallow trench isolation (STI) structure and controlling the distance from the STI to the transistor channels (paragraphs 0247 - 0252). The seventh embodiment provides stress to the transistor channels from stressed films forming sidewalls on the gate rather than developing stresses in the gate structure itself (paragraphs 0261 - 0265).

Thus, it is seen that while Kumagai et al. is directed to adjustment of carrier mobility by applying stress to the transistor channel, Kumagai et al. does not teach (or suggest) developing such stress by forming stressed alloy (or "silicide" as used in the sense described ast page 13, lines 13 - 16 of the present specification) in the gate structure. It appears that Kumagai et al. does not even recognize the possibility of doing so in view of the teaching of silicide film 17 to which no stress generation or transfer is attributed and the teaching of using silicide of controlled thickness in the source and

drain regions of a transistor but not in the gate structure thereof.

Accordingly, it is seen that Kumagai et al. does not, in fact, answer the explicit recitations of claim 1 and thus does not anticipate any claim in the application. Likewise, Kumagai et al. does not teach (or suggest) the subject matter of dependent claims such as, for example, depositing metal over one gate structure and not over another or applying alloys developing opposing stresses as recited in claims 4 and 5. In the third embodiment, which is the only embodiment even arguably (and then only inferentially) developing stress in a silicide, stress is controlled by differential silicide thickness.

It is also respectfully submitted, for the reasons discussed above, that Kumagai et al. does not provide evidence of a level of ordinary skill in the art which would support a conclusion of obviousness in regard to the subject matter of any claim. *It is believed to be highly significant in this regard that the fourth and fifth embodiments of Kumagai et al., the only embodiments in which stresses are transferred from the gate structure to the transistor channel, that the stresses are developed from ion implantation or grain size manipulation but not from silicide formation. That is, the fourth and fifth embodiments clearly appear (especially if it is assumed, arguendo, that the silicide in the source and drain regions of the third embodiment is a stressed silicide) to infer that Kumagai et al. has not even conceived of the possibility of developing a silicide structure in a transistor gate which could transfer stress to the transistor channel or a method of forming such a structure, and, indeed, such a structure as provided by the invention is not intuitive and may involve close process controls such as are disclosed, for example, on page 14, lines 6 - 19.* Therefore, Kumagai et al.

clearly does not lead to an expectation of success in achieving enhancement of carrier mobility by silicide formation in a transistor gate structure, as claimed, much less doing so for single transistors or in a complementary fashion for transistors of opposite conductivity types.

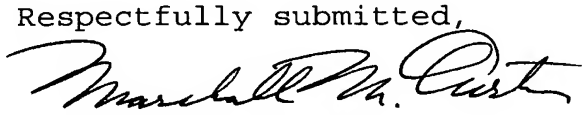
Accordingly, it is respectfully submitted that the rejection of claims 1 - 7 for anticipation by Kumagai et al. is clearly in error and untenable. Further, even in view of the wide variety of embodiments disclosed by Kumagai et al., Kumagai et al. does not suggest the claimed invention or provide evidence of a level of ordinary skill in the art which would support a conclusion of obviousness of the subject matter of any claim. Further, in regard to both anticipation and obviousness the Examiner's statement of the rejection appears, at best, to merely address the "gist" of the invention but not the actual claimed subject matter. Such a statement of a ground of rejection is clearly well-established to be insufficient to make a *prima facie* demonstration of either anticipation or obviousness. See, for example, M.P.E.P. §2141.02. Therefore, reconsideration and withdrawal of the sole ground of rejection of claims 1 - 7 and the allowance of the application are respectfully requested.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that this application is in condition for allowance and such action is therefore respectfully requested.

If an extension of time is required for this response to be considered as being timely filed, a

conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to International Business Machine Deposit Account No. 09-0458.

Respectfully submitted,



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